automatically adjusting at least one of a frequency component and a phase component of the pixel clock signal until E equals W.

5. The method of claim 4, including the steps of:

automatically determining whether a phase difference exists between the pixel clock signal and the analog video data signal; and

automatically shifting the pixel clock phase to substantially eliminate the phase difference.

6. The method of claim 4, wherein the actual width W is equal to an actual number of pixel clocks from an actual left-most active pixel clock in a frame that reads a left-most actual active portion of the analog video data signal in the frame, to an actual right-most pixel clock in the frame that reads a right-most actual active portion of the analog video data signal in the frame.

7. The method of claim 6, wherein the expected width E is equal to an expected number of pixel clocks from an expected left-most pixel clock in the frame that reads an expected left-most active portion of the analog video data signal in the frame, to an expected right-most pixel clock in the frame that reads an expected right-most active value of the analog video data signal in the frame.

8. The method of claim 7, wherein the frequency component of the pixel clock signal is adjusted whenever one of W>E+1 and W<E holds true in the frame.

9. The method of claim 7, wherein the frequency component of the pixel clock signal is decreased whenever E<W−1.

10. The method of claim 7, wherein the frequency component of the pixel clock signal is increased whenever E>W.

11. The method of claim 4, wherein the frequency component of the pixel clock signal is adjusted by adjusting a number *n* of pixel clocks across each line in a frame of the analog video data signal.

12. The method of claim 11, wherein the number *n* of pixel clocks and the expected width E are determined by reference to a look-up table.

13. The method of claim 4, wherein the frequency component of the pixel clock signal is adjusted before the phase component of the pixel clock signal is adjusted.

14. The method of claim 4, wherein the phase of the pixel clock signal is adjusted by the steps:

adjusting the pixel clock signal phase by a selected iterative amount for each of a series of subsequent frames until a frame phase error condition passes from W=E+1 through a subseries of frames where W=E, and back to a frame with a phase error condition of W=E+1;

storing the W values from the series of subsequent frames;

examining the W values to identify the subseries of consecutive frames in which W=E;

selecting a phase corrected frame in a center portion of the subseries of frames; and

setting the pixel clock phase at the phase of the phase corrected frame.

15. A method for recovering a correct phase and frequency clock for an analog video signal that is converted for display on a digital display object having pixels arranged in lines and columns, the analog video signal including an analog video data signal that is operable for raster scanning in lines across a CRT screen to form consecutive frames of video information, the raster scanning controlled by timing signals that control a line scan rate and a frame refresh rate, to produce consecutive frames of video information, comprising the steps of:

generating a pixel clock signal that reads instantaneous values of the analog video data signal;

setting a total number *n* of pixel clocks that read the analog video data signal along each horizontal line;

determining an expected number E of pixel clocks from an expected left-most pixel clock in a frame that reads a left-most value of the analog video data signal that is greater than a selected threshold value, to an expected right-most pixel clock in the frame that reads a right-most value of the analog video data signal that is greater than the selected threshold value, the expected number E indicating an expected width of active analog video data;

determining an actual number W of pixel clocks from an actual left-most active pixel clock in the frame that reads a left-most actual value of the analog video data signal that is greater than the selected threshold value, to an actual right-most pixel clock in the frame that reads a right-most actual value of the analog video data signal that is greater than the selected threshold value, the actual number W indicating an actual width of active analog video data; and

comparing the actual number W with the expected number E.

16. The method of claim 15, including the steps of:

when one of W>E+1 and W<E, calculating an adjusted total number *n'* of pixel clocks that read instantaneous analog video data signal values across each line of analog video signal=*n*·(E/W);

substituting *n'* for *n* for a next frame; and

redetermining the actual number W of pixel clocks for the next frame.

17. The method of claim 15, including the steps of:

when W=E+1, adjusting pixel clock signal phase for a next frame; and

redetermining the actual number W of pixel clocks for the next frame.

18. The method of claim 15, including the steps of:

when W=E+1, adjusting pixel clock signal phase by a selected iterative amount for each of a series of subsequent frames;

determining the actual number W of pixel clocks for each of the series of subsequent frames; and

storing the actual number W of pixel clocks for each of the series of subsequent frames;

identifying a subseries of consecutive frames in which W=E;

selecting a corrected frame from the subseries of consecutive frames, the corrected frame being from a middle portion of the subseries of consecutive frames;

identifying a corrected pixel clock signal phase of the corrected frame; and

setting the pixel clock signal phase to the corrected pixel clock signal phase.

19. The method of claim 15, including the step of correlating the expected width of the video image to an expected number E of pixel clocks.

20. The method of claim 15, including the step of correlating the actual width of the video image to an actual number W of activated pixels.

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21. A method for recovering a correct phase and frequency clock for an analog video signal that is converted into a digital video signal for display on a digital display object having pixels arranged in lines and columns, the analog video signal including an analog video data signal that is operable for raster scanning in lines across a display screen to form consecutive frames of video information, the raster scanning controlled by timing signals that control a line scan rate and a frame refresh rate to produce consecutive frames of video information, comprising:

estimating an expected width of an image producible by the analog video signal;

determining an actual width of an image producible by the digital video signal; and

iteratively adjusting the digital video signal until the actual width equals the expected width.

22. The method of claim 21, further including:

generating a pixel clock signal that samples the analog video signal to convert the analog video signal to the digital video signal; and

iteratively adjusting at least one of frequency and phase of the pixel clock signal to iteratively adjust the digital video signal.

23. The method of claim 22, further including adjusting the frequency of the pixel clock signal before adjusting the phase of the pixel clock signal.

24. The method of claim 21, in which the determining an actual width of an image includes determining a difference between a number of reference clock counts occurring between successive sync pulses associated with the lines of the digital display object and a number of reference clock counts occurring within a blanked data interval between next successive sync pulses associated with a line of the display object.

25. The method of claim 24, in which the number of reference clock counts occurring between successive sync pulses represents for each line of the digital display object an average number of clock counts taken over multiple sync pulses.